

PATENT ABSTRACTS OF JAPAN

(11) Publication number:

55118153 A

(43) Date of publication of application:

COPYRIGHT: (C)1980,JPO&Japio

10 . 09 . 80

(51) Int. CI

G06F 9/30 G06F 7/00

(21) Application number: 54025289

(22) Date of filing: 05 . 03 . 79

(71) Applicant:

NEC CORP

(72) Inventor:

KADOTA HIROSHI MIURA KATSUMI

(54) OPERATION PROCESSOR

(57) Abstract:

PURPOSE: To increase the processing speed by giving the NOP (operation) action when the coincidence of the contents is obtained between the signal source field and the result storage destination field and at the same time transmitting the data possessed by the register to other process control part as well.

CONSTITUTION: The unit which executes register transfer orders MOVR_i and R_k possesses comparator circuit 7 which gives the comparison to the contents between the signal source field and the result storage destination field. For circuit 7, bit signals $\mathsf{SC}_1\mathsf{WSC}_n$ forming the signal field plus bit signals $\mathsf{DS}_1\mathsf{WDS}_n$ forming the result storage destination field are connected to the input ends of n units of exclusive NOR gate 10. And the output is supplied to AND gate 11 to deliver coincidence signal 12. When the coincidence of the contents is obtained between the both field, i.e., $\mathsf{R}_i{=}\mathsf{R}_k$ is obtained, the coincidence signal is sent to gate circuit 8. Circuit 8 sends the data from register R_i to register R_k and also transfers to other process mechanism.



